1. A pulse clock/signal delay apparatus (PCD) comprising;

a series-connected chain of N pulse delay stages, $1 \leq N \leq Nmax$, each stage having an input and respective output with a pulse delay of Δt therebetween, the pulse delay stages connected output to following input from a first stage (N=1) to a next-to-last stage (N=Nmax -1);

an input of the apparatus connected to an input of the first stage (N = 1) of the N pulse delay stages;

an output of the apparatus connected to an output of an Nd-th stage ($N = Nd \leq Nmax$), of the N pulse delay stages by a Diagonal Cross Point matrix (400), having;

M parallel and spaced apart row select input lines (402[m]) each connected separately at an outer peripheral end to a corresponding one of M row access select (RAS) lines (xr[m]) of a matrix select bus (240);

N parallel and spaced apart column select input lines (404[n]), each connected separately at an outer peripheral end to a corresponding one of N column access select CAS lines (yc[n]) of the matrix select bus (240) in which the M row lines (402[m]) are not parallel to the N column lines (404[n]) and both the RAS lines and the CAS lines are directed proximally away from the respective outer peripheral ends toward one side of a diagonal (500) disposed from opposite corners (C1, C3) of the diagonal cross point (DCP) (400);

Nmax parallel and spaced apart column delay signal input lines (406[j]), each separately connected at a respective outer peripheral end to a corresponding one of delayed signal outputs (213[j]) from a series delay block (260);

Nmax parallel and spaced apart row switch outputs lines (409[j]) each separately connected at a respective outer peripheral end to corresponding matrix outputs xout[j], where M = N = Nmax and the column delay signal input lines (406[j]) are not parallel to the row switch output lines (409(j]) and the column delay signal input lines and the row switch output lines are both directed proximally from respective outer peripheral ends toward the opposite side of the diagonal (500);

2. A pulse clock/signal delay apparatus as claimed in claim 1, wherein,
the row select input lines (402[j]) and row switch output lines (409[j]) of the diagonal cross point matrix are mutually aligned.

3. A pulse clock/signal delay apparatus as claimed in claim 1, wherein,
the row select input lines (402[j]) and row switch output lines (409[j]) of the diagonal cross point matrix are mutually offset.

4. A pulse clock/signal delay apparatus as claimed in claim 1 wherein,
the column input signal lines (406[j]) and column select input lines (404[j]) of the diagonal cross point matrix are mutually aligned.

5. A pulse clock/signal delay apparatus as claimed in claim 1, wherein,
the column input signal lines (406[j]) and column select input lines (404[j]) of the diagonal cross point matrix are mutually offset.

6. A pulse clock/signal delay apparatus as claimed in claim 1, wherein in the diagonal cross point matrix,
an array of switches (sx[j]) is disposed generally along the diagonal 500 across the DCP 400 with a switch (sx[j]) at each intersection of row (402[m=j]) and column (404[n=j]);
each switch (sx[j]) has a respective row input (402[j]) and column input (404[j]) of a two input AND gate (410[j]) disposed essentially at the intersection of row m and column n only where m=n=j; and
the AND gate (410[j]) drives a base input (412[j]) of an adjacent NPN transistor switch (414(j]) that has its collector (416[j]) connected to an opposite proximal end of the corresponding column delay signal input line (406[j]) and its emitter (418[j]) connected to the corresponding opposite proximal end of the row switch output (409[j]).

7. A pulse clock/signal delay apparatus as claimed in claim 6, wherein in the diagonal cross point matrix,

a logic '1' is required in both of an AND operation of row gate inputs (402[j]) and column gate inputs (404(j]) to form an electrical connection between a column (406[j]) and row (409[j]).

8. A pulse clock/signal delay apparatus as claimed in claim 6, wherein;

the column address select (CAS) signals (404[n]) (from yc[n]) and row address select (RAS) signals (402[m]) (from xr[m]) are separated from the delayed clock signals (406[j]) and switched output signals (xout[j]) by a spatial separation except for their end-to-end proximity near the AND inputs (402[j] and 404[j]) at the diagonal (500).

9. A pulse clock/signal delay apparatus as claimed in claim 8, wherein;

the spatial separation tends to minimise coupling between the column address select (CAS) signals (404[n]) and row address select (RAS) signals (402[m]) and the delayed clock signals (406[j]) and switched output signals (xout[j]) thereby tending to improve isolation between control and signal data.

10. A pulse clock/signal delay apparatus (PCD) comprising;

a series-connected chain of N pulse delay stages, $1 \leq N \leq$ Nmax, each stage having an input and respective output with a pulse delay of Δt therebetween, the stages connected output to following input from a first stage (N = 1) to a next-to-last stage (N=Nmax -1);

an input of the apparatus connected to an input of the first stage (N = 1) of the N pulse delay stages;

an output of the apparatus connected to an output of an Nd-th stage ($N = Nd \leq$ Nmax) of the N pulse delay stages by a Diagonal Cross Point matrix (400), having:

M parallel and spaced apart row select input lines (402[m]) each connected separately at an outer peripheral end to a corresponding one of M row access select (RAS) lines (xr[m]) of a matrix select bus (240);

N parallel and spaced apart column select input lines (404[n]), each connected separately at an outer peripheral end to a corresponding one of N column access select (CAS) lines (ye[n]) of matrix select bus (240) in which the M row lines (402[m]) are not parallel to the N column lines (404[n]) and both the RAS lines and the CAS lines are directed proximally away from the respective outer peripheral ends toward one side of a diagonal (500) disposed from opposite corners (C1, C3) of the diagonal cross point (DCP) (400);

Nmax parallel and spaced apart column delay signal input lines (406[j]), each separately connected at a respective outer peripheral end to a corresponding one of delayed signal outputs (213[j]) from a series delay block (260);

Nmax parallel and spaced apart row switch outputs lines (409[j]) each separately connected at a respective outer peripheral end to corresponding matrix outputs xout[j], where M = N = Nmax and the column delay signal input lines (406[j]) are not parallel to the row switch output lines (409[j]) and the column delay signal input lines and the row switch output lines are both directed proximally from respective outer peripheral ends toward the opposite side of the diagonal (500); and

an array of switches (sx[j]) is disposed generally along the diagonal 500 across the DCP 400 with a switch (sx[j]) at each intersection of row (402[m=j]) and column (404[n=j]), each switch (sx[j]) having a respective row input (402[j]) and column input (404[j]) of a two input AND gate (410[j]) disposed essentially at the intersection of row m and column n only where m=n=j; and the AND gate (410[j]) driving a switching input (412[j]) of a device selected from the group of an N-channel FET, and a PNP transistor with inverted logic levels and a P-channel FET with inverted logic levels that has an input (416[j]) connected to an opposite proximal end of the corresponding column delay signal input line (406[j]) and an output (418[j]) connected to the corresponding opposite proximal end of the row switch output (409[j]).

11. A pulse clock/signal delay apparatus (PCD) comprising:

a series-connected chain of N pulse delay stages, $1 \leq N \leq Nmax$, each stage having an input and respective output with a pulse delay of Δt therebetween, the stages connected output to following input form a first stage (N=1) to a next-to-last stage (N=Nmax -1);

an input of the apparatus connected to an input of the first stage (N = 1) of the N pulse delay stages; and

an output of the apparatus connected to an output of an Nd-th stage ($N = Nd \leq Nmax$) of the N pulse delay stages by a Diagonal Cross Point matrix (400), having:

M parallel and spaced apart row select input lines (402[m]) each connected separately at an outer peripheral end to a corresponding one of M row access select (RAS) lines (xr[m]) of a matrix select bus (240);

N parallel and spaced apart column select input lines (404[n]), each connected separately at an outer peripheral end to a corresponding one of N column access select (CAS) lines (ye[n]) of matrix select bus (240) in which the M row lines (402[m]) are not parallel to the N column lines (404[n]) and both the RAS lines and the CAS lines are directed proximally away from the respective outer peripheral ends toward one side of a diagonal (500) disposed from opposite corners (C1, C3) of the diagonal cross point (DCP) (400);

Nmax parallel and spaced apart column delay signal input lines (406[j]), each separately connected at a respective outer peripheral end to a corresponding one of delayed signal outputs (213[j]) from a series delay block (260);

Nmax parallel and spaced apart row switch outputs lines (409[j]) each separately connected at a respective outer peripheral end to corresponding matrix outputs xout[j], where M = N = Nmax and the column delay signal input lines (406[j]) are not parallel to the row switch output lines (409[j]) and the column delay signal input lines and the row switch output lines are both directed proximally from respective outer peripheral ends toward the opposite side of the diagonal (500); and

an array of switches (sx[j]) disposed generally along the diagonal 500 across the DCP 400 with a switch (sx[j]) at each intersection of row (402[m=j]) and column (404[n=j]), each switch (sx[j]) having a respective row input (402[j]) disposed essentially at the intersection of row m and column n only where m=n=j, the AND gate (410[j]) disposed essentially at the intersection of row m and column n only where m=n=j, the AND gate (410[j]) driving a switching input (412[j]) of a programmable fixed connection device selected from the group of an EEPROM programmable FET, a programmable metal fuse and a programmable anti-fuse that has an input (416[j]) connected to an opposite proximal end of the corresponding column delay signal input line (406[j]) and an output (518[j]) connected to the corresponding opposite proximal end of the row switch output (409[j]).

12. A pulse clock/signal delay apparatus as claimed in claim 1, wherein a plurality of switches is selectable by each combination of a row select input line (402[m]) and column select input line (404[n]).

13. A pulse clock/signal delay network (200) having a first signal path, (S1[p]) and a second signal path (S2[p]) wherein the first signal path and second signal path have a common end for receiving a pulse edge (102), and the second signal path (S2[p]) is electrically longer than first signal path (S1[p]) by a time delay tdel, such that the pulse edge (102) propagates through the second path (S2[p]) to a distal end of the second path to arrive at a second time instance t2, and the pulse edge (102) propagates through the first pat (S1[p]) to a distal end of the first path to arrive at first time instance t1, the difference between t2 and t1 being tdel, said pulse clock/signal delay network comprising:

a series-connected chain of N pulse delay stages, $1 \leq N \leq Nmax$, each stage having an input and respective output with a pulse delay of Δt therebetween, the pulse delay stages connected output to following input from a first stage (N=1) to a next-to-last stage (N=Nmax -1), located between an intermediate node (n1a) and an adjacent intermediate note (n1b) formed in the first path (S1[p]) by separating the first path (S1[p]) at a node (n1) between the common end and the distal end of

the first path (S1[p]) into a first path segment (S1a[p]) from the common end to the intermediate node (n1a) and a second path segment (S1b[p]) between the adjacent intermediate node (n1b) an the distal end of the first path (S1[p]);
an input of the first stage (N = 1) being connected to the intermediate node (n1a); and
an output of an Nd-th stage (N = Nd ≤ Nmax) being connected to the adjacent intermediate node (n1b) such that $|tdel - Nd*\Delta t| \leq \Delta t$, by a connecting switch comprising a Diagonal Cross Point matrix (400), having:
M parallel and spaced apart row select input lines (402[m]) each connected separately at an outer peripheral end to a corresponding one of M row access select (RAS) lines (xr[m]) of a matrix select bus (240);
N parallel and spaced apart column select input lines (404[n]), each connected separately at an outer peripheral end to a corresponding one of N column access select (CAS) lines (ye[n]) of the matrix select bus (240) in which the M row lines (402[m]) are not parallel to the N column lines (404[n]) and both the RAS lines and the CAS lines are directed proximally away from the respective outer peripheral ends toward one side of a diagonal (500) disposed from opposite corners (C1, C3) of the diagonal cross point (DCP) (400);
Nmax parallel and spaced apart column delay signal input lines (406[j]), each separately connected at a respective outer peripheral end to a corresponding one of delayed signal outputs (213[j]) from a series delay block (260);
Nmax parallel and spaced apart row switch outputs lines (409[j]) each separately connected at a respective outer peripheral end to corresponding matrix outputs xout[j], where M = N = Nmax and the delay signal input column lines (406[j]) are not parallel to the row switch output lines (409[j]) and the column delay signal input lines and the row switch output lines are both directed proximally from respective outer peripheral ends toward the opposite side of the diagonal (500);
whereby the pulse edge (102) propagates through the series connection of path segment S1a[p], the Nd pulse delay stages, and path segment (S1b[p]) to arrive at a time instance t1', where $|t2 - t1'| \leq \Delta t$.

14. A pulse clock/signal delay apparatus (PCD) comprising:

a series-connected chain of N pulse delay stages, $1 \leq N \leq Nmax$, each stage having an input and respective output with a pulse delay of Δt therebetween, the pulse delay stages connected output to following input from a first stage (N=1) to a next-to-last stage (N=Nmax 01);

an input of the apparatus connected to an input of the first stage (N = 1) of the N pulse delay stages;

an output of the apparatus connected to an output of an Nd-th stage ($N = Nd \leq Nmax$) of the N pulse delay stages by a Diagonal Cross Point matrix (400), having:

M parallel and spaced apart row select input lines (402[m]) each connected separately at an outer peripheral end to a corresponding one of M row access select (RAS) lines (xr[m]) of a matrix select bus (240);

N parallel and spaced apart column select input lines (404[n]), each connected separately at an outer peripheral end to a corresponding one of N column access select (CAS) lines (ye[n]) of the matrix select bus (240) in which the M row lines (402[m]) are not parallel to the N column lines (404[n]) and both the RAS lines and the CAS lines are directed proximally away from the respective outer peripheral ends toward one side of a diagonal (500) disposed from opposite corners (C1, C3) of the diagonal cross point (DCP) (400);

Nmax parallel and spaced apart column delay signal input lines (406[j]), each separately connected at a respective outer peripheral end to a corresponding one of delayed signal outputs (213[j]) from a series delay block (260);

Nmax parallel and spaced apart row switch output lines (409[j]) each separately connected at a respective outer peripheral end to corresponding matrix outputs xout[j], where M = N = Nmax and the column delay signal input lines (406[j]) are not parallel to the row switch output lines (409[j]) and the column delay signal input lines and the row switch output lines are both directed proximally from respective outer peripheral ends toward the opposite side of the diagonal (500); and

an array of switches (sx[j]) disposed generally along the diagonal 500 across the DCP 400 with a switch (sx[j]) at each intersection of row (402[m=j]) and column 404[n=j]), each switch (sx[j]) having a respective row input (402[j]) and column input (404[j]) of a two input AND gate (410[j]) disposed essentially at the intersection of row m and column n only where m=n=j, the AND gate (410[j]) driving a base input (412[j]) of an adjacent NPN transistor switch (414[j]) that has its collector (416[j]) connected to an opposite proximal end of the corresponding column delay signal input line (406[j]) and its emitter (418[j]) connected to the corresponding opposite proximal end of the row switch output (409[j]).

15. A pulse clock/signal delay apparatus as claimed claim 13, wherein in the diagonal cross point matrix, a logic '1' is required in both of an AND operation of row gate inputs (402[j]) and column gate inputs (404[j]) to form an electrical connection between a column (406[j]) and row (409[j]).

16. A pulse clock/signal delay apparatus as claimed in claim 13, wherein the column address select (CAS) signals (404[n]) (from ye[n]) and row address select (RAS) signals (402[m]) (from xr[m]) are separated from the delayed clock signals (406[j]) and switched output signals (xout[j]) by a spatial separation except for their end-to-end proximity near the AND inputs (402[j] and 404[j] at the diagonal (500).

17. A pulse clock/signal delay apparatus as claimed in claim 8, wherein the spatial separation tends to minimise coupling between the column address select (CAS) signals (404[n]) and row address select (RAS) signals (402[m]) and the delayed clock signals (46[j]) and switched output signals (xout[j]) thereby tending to improve isolation between control and signal data.